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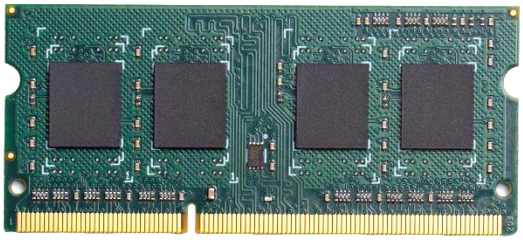
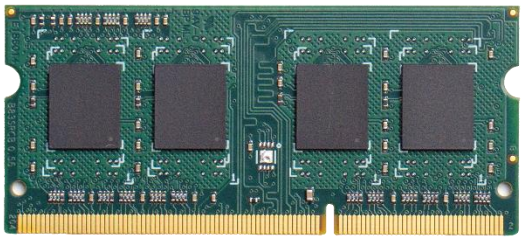
4GB DDR3-1600 SO-DIMM 1.35V

204pin PC3-12800 DDR3L Unbuffered SO-DIMM Non-ECC





TEL:+886-3-3465059 FAX:+886-3-3467059
4F., No.890 Jingguo Rd., Luzhu Dist., Taoyuan City 338, Taiwan
AlfaMemory Technology Co., Ltd.

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TEL:+886-3-3465059 FAX:+886-3-3467059
4F., No.890 Jingguo Rd., Luzhu Dist., Taoyuan City 338, Taiwan
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AMC045MBDPB8

4G Bytes (512M x 64 bits)
based on 8 pcs 512M x 8 DDR3L SDRAM
204pin PC3-12800 DDR3L Unbuffered SO-DIMM Non-ECC

Specifications

- RoHS Compliant (Lead Free) Memory module
- Density: 4GB
- Organization
  — 512M x 64 bits, 1 Rank
- Mounting 8 pieces of 4G bits DDR3L SDRAM sealed In FBGA
- Package: 204-pin socket type Unbuffered dual in line memory module (SODIMM)
  — PCB height: 30.00mm
- VDD = 1.35V (1.283V to 1.45V)
- VDDSPD = +3.0V to +3.6V
- Backward Compatible with 1.5V DDR3 Memory module
- Fast Data Transfer Rate: PC3-12800
- Serial Presence-Detect (SPD)with EEPROM
- Eight Internal banks for concurrent operation (components)
- On-Die-Termination (ODT) for better signal quality
- Interface: SSTL_15
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- CAS (READ) latency (CL): 5, 6, 7, 8, 9, 10, 11
- POSTED CAS ADDITIVE latency (AL)
- Precharge: Auto precharge option for each burst access
- Refresh: Auto-refresh, self-refresh
- T_{CASE} of 0°C to 95°C (Components)
  — 64ms, 8,192 cycle refresh at 0°C to 85°C — 32ms at 85°C to 95°C
- Operating Temperature
  — T_{OPR} (Tcase) = 0°C to +85°C
- Fly-by topology

Features

- Double-data-rate architecture; two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted /CAS by progrmmable additive latency for better command and data bus efficiency
- On-Die-Termination (ODT) for better signal quality
  — Synchronous ODT — Dynamic ODT
  — Asynchronous ODT
- Multi Purpose Register (MPR) for temperature read out
- ZQ calibration for DQ drive and ON-Die-Termination
- Progrmmable Partial Array Self-Refresh (PASR)
- /RESET pin for Power-up sequence and reset function • Extended Self-Refresh — External Self-Refresh — Auto Self-Refresh

Key Parameters

MT/s	tCK (ns)	CAS Latency (tCK)	tRCD (ns)	tRP (ns)	tRAS (ns)	tRC (ns)	CL-tRCD-tRP
DDR3-1600	1.25	11	13.125	13.125	35	48.125	11-11-11

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Pin Descriptions

Pin Name	Description	Number	Pin Name	Description	Number
CK0, CK1	Clock Inputs, positive line	2	DQ0-DQ63	Data Input/Output	64
CK0, CK1	Clock Inputs, negative line	2	DM0-DM7	Data Masks/ Data strobes, Termination data strobes	8
CKE0, CKE1	Clock Enables	2	DQS0-DQS7	Data strobes	8
RAS	Row Address Strobe	1	DQS0-DQS7	Data strobes complement	8
CAS	Column Address Strobe	1	RESET	Reset Pin	1
WE	Write Enable	1	TEST	Logic Analyzer specific test pin (No connect on SODIMM)	1
S0, S1	Chip Selects	2	V_{DD}	Core and I/O Power	18
A0-A9, A11, A13-A15	Address Inputs	14	V_{SS}	Ground	52
A10/AP	Address Input/Autoprecharge	1	V_{REFDQ} V_{REFCA}	Input/Output Reference	2
A12/BC	Address Input/Burst chop	1	V_{DDSPD}	SPD and Temp sensor Power	1
BA0-BA2	SDRAM Bank Addresses	3	V_{TT}	Termination Voltage	2
ODT0, ODT1	On-die termination control	2	NC	Reserved for future use	3
SCL	Serial Presence Detect (SPD) Clock Input	1		Total	204
SDA	SPD Data Input/Output	1			
SA0-SA1	SPD Address	2			

NOTE:
* The V_{DD} and V_{DDQ} pins are tied common to a single power-plane on these designs.

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Input/Output Functional Descriptions

Symbol	Type	Function
CK0-CK1 CK0-CK1	Input	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of CK. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE0-CKE1	Input	Activates the DDR3 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{S}0$-$\overline{S}1$	Input	Enables the associated DDR3 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{S}0$; Rank 1 is selected by $\overline{S}1$.
RAS, CAS, WE	Input	When sampled at the cross point of the rising edge of CK and falling edge of CK, signals CAS, RAS, and WE define the operation to be executed by the SDRAM.
BA0-BA2	Input	Selects which DDR3 SDRAM internal bank of eight is activated.
ODT0-ODT1	Input	Asserts on-die termination for DQ, DM, DQS, and DQS signals if enabled via the DDR3 SDRAM mode register.
A0-A9, A10/AP, A11 A12/BC A13-A15	Input	During a Bank Activate command cycle, defines the row address when sampled at the cross point of the rising edge of CK and falling edge of CK. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of CK. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is low, then BA0-BAn are used to define which bank to precharge.A12(BC) is sampled during READ and WRITE commands to determine if burst chop (on-the fly) will be performed (HIGH, no burst chop; LOW, burst chopped)
DQ0-DQ63	I/O	Data Input/Output pins.
DM0-DM7	Input	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
DQS0-DQS7 DQS0-DQS7	I/O	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR3 SDRAMs and is sent at the leading edge of the data window. DQS signals are complements, and timing is relative to the crosspoint of respective DQS and DQS.
V_{DD},V_{DDSPD}, V_{SS}	Supply	Power supplies for core, I/O, Serial Presence Detect, Temp sensor, and ground for the module.
V_{REFDQ}, V_{REFCA}	Supply	Reference voltage for SSTL15 inputs.
SDA	I/O	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM and Temp sensor. A resistor must be connected from the SDA bus line to V_{DDSPD} on the system planar to act as a pull up.
SCL	Input	This signal is used to clock data into and out of the SPD EEPROM and Temp sensor.
SA0-SA1	Input	Address pins used to select the Serial Presence Detect and Temp sensor base address.
TEST	I/O	The TEST pin is reserved for bus analysis tools and is not connected on normal memory modules
RESET	Input	RESET In Active Low This signal resets the DDR3 SDRAM

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Pin Configurations

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VREFDQ	2	VSS	71	VSS	72	VSS	139	VSS	140	DQ38
3	VSS	4	DQ4	KEY				141	DQ34	142	DQ39
5	DQ0	6	DQ5	73	CKE0	74	CKE1	143	DQ35	144	VSS
7	DQ1	8	VSS	75	VDD	76	VDD	145	VSS	146	DQ44
9	VSS	10	DQS0	77	NC	78	A15[3]	147	DQ40	148	DQ45
11	DM0	12	DQS0	79	BA2	80	A14[3]	149	DQ41	150	VSS
13	VSS	14	VSS	81	VDD	82	VDD	151	VSS	152	DQS5
15	DQ2	16	DQ6	83	A12/BC	84	A11	153	DM5	154	DQS5
17	DQ3	18	DQ7	85	A9	86	A7	155	VSS	156	VSS
19	VSS	20	VSS	87	VDD	88	VDD	157	DQ42	158	DQ46
21	DQ8	22	DQ12	89	A8	90	A6	159	DQ43	160	DQ47
23	DQ9	24	DQ13	91	A5	92	A4	161	VSS	162	VSS
25	VSS	26	VSS	93	VDD	94	VDD	163	DQ48	164	DQ52
27	DQS1	28	DM1	95	A3	96	A2	165	DQ49	166	DQ53
29	DQS1	30	RESET	97	A1	98	A0	167	VSS	168	VSS
31	VSS	32	VSS	99	VDD	100	VDD	169	DQS6	170	DM6
33	DQ10	34	DQ14	101	CK0	102	CK1	171	DQS6	172	VSS
35	DQ11	36	DQ15	103	CK0	104	CK1	173	VSS	174	DQ54
37	VSS	38	VSS	105	VDD	106	VDD	175	DQ50	176	DQ55
39	DQ16	40	DQ20	107	A10/AP	108	BA1	177	DQ51	178	VSS
41	DQ17	42	DQ21	109	BA0	110	RAS	179	VSS	180	DQ60
43	VSS	44	VSS	111	VDD	112	VDD	181	DQ56	182	DQ61
45	DQS2	46	DM2	113	WE	114	S0	183	DQ57	184	VSS
47	DQS2	48	VSS	115	CAS	116	ODT0	185	VSS	186	DQS7
49	VSS	50	DQ22	117	VDD	118	VDD	187	DM7	188	DQS7
51	DQ18	52	DQ23	119	A13[3]	120	ODT1	189	VSS	190	VSS
53	DQ19	54	VSS	121	S1	122	NC	191	DQ58	192	DQ62
55	VSS	56	DQ28	123	VDD	124	VDD	193	DQ59	194	DQ63
57	DQ24	58	DQ29	125	TEST	126	VREFCA	195	VSS	196	VSS
59	DQ25	60	VSS	127	VSS	128	VSS	197	SA0	198	NC
61	VSS	62	DQS3	129	DQ32	130	DQ36	199	VDDSPD	200	SDA
63	DM3	64	DQS3	131	DQ33	132	DQ37	201	SA1	202	SCL
65	VSS	66	VSS	133	VSS	134	VSS	203	VTT	204	VTT
67	DQ26	68	DQ30	135	DQS4	136	DM4				
69	DQ27	70	DQ31	137	DQS4	138	VSS				

NOTE : 1. NC = No Connect, NU = Not Used, RFU = Reserved Future Use
2. TEST(pin 125) is reserved for bus analysis probes and is NC on normal memory modules.
3. This address might be connected to NC balls of the DRAMs (depending on density); either way they will be connected to the termination resistor.

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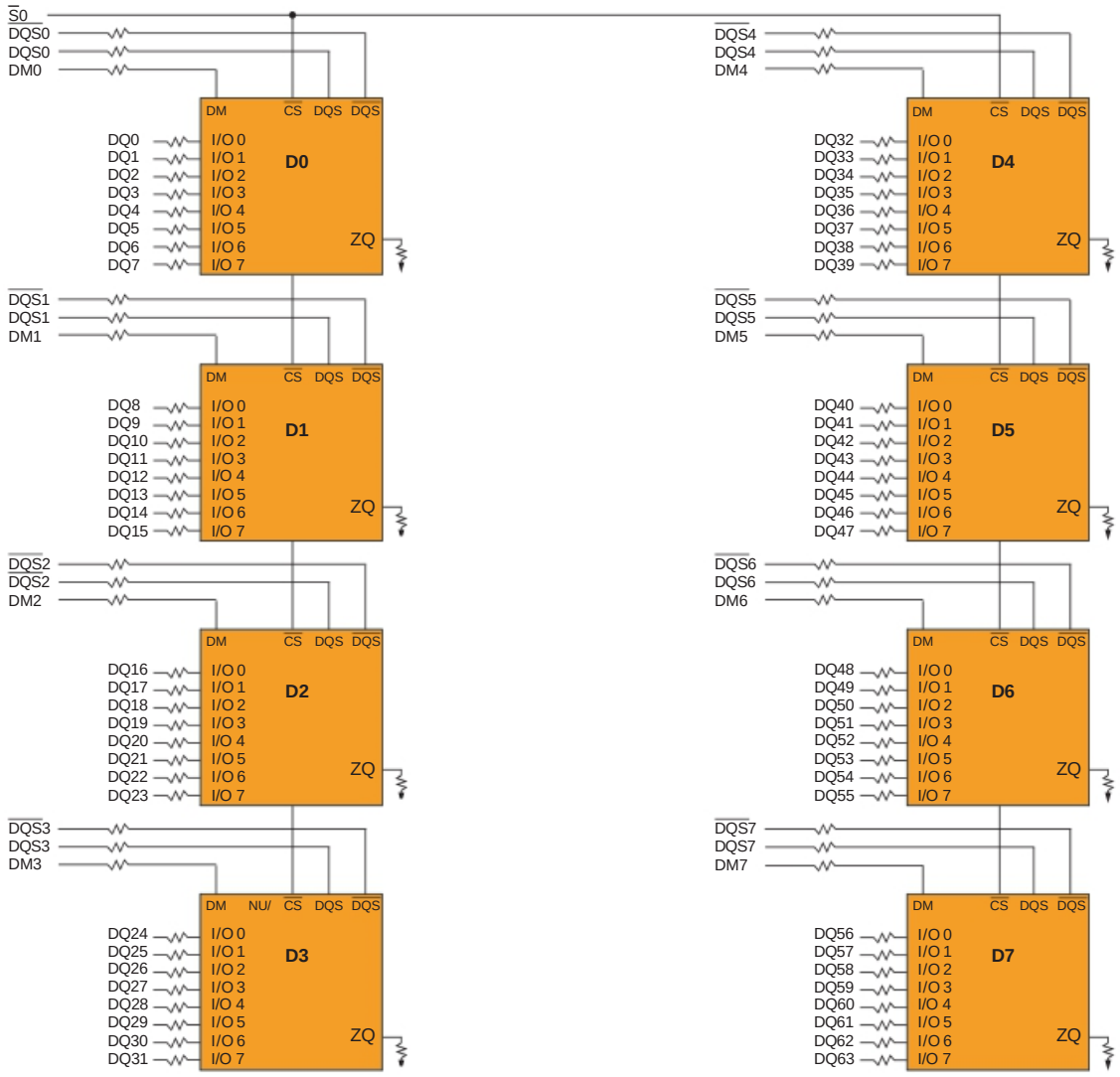
Functional Block Diagram



BA0 - BA2 → BA0-BA2 : SDRAMs D0 - D15

A[15/14/13:0] → A[15/14/13:0] : SDRAMs D0 - D15

CKE1 → CKE : SDRAMs D8 - D15

CKE0 → CKE : SDRAMs D0 - D7

$\overline{RAS}$ → $\overline{RAS}$: SDRAMs D0 - D15

$\overline{CAS}$ → $\overline{CAS}$: SDRAMs D0 - D15

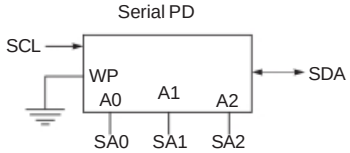
$\overline{WE}$ → $\overline{WE}$: SDRAMs D0 - D15

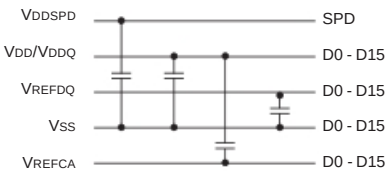
ODT0 → ODT : SDRAMs D0 - D7

ODT1 → ODT : SDRAMs D8 - D15

CK0 → CK : SDRAMs D0 - D7

CK1 → CK : SDRAMs D8 - D15





NOTE :

1. For each DRAM, a unique ZQ resistor is connected to ground. The ZQ resistor is 240 Ohm +/- 1%
2. One SPD exists per module.

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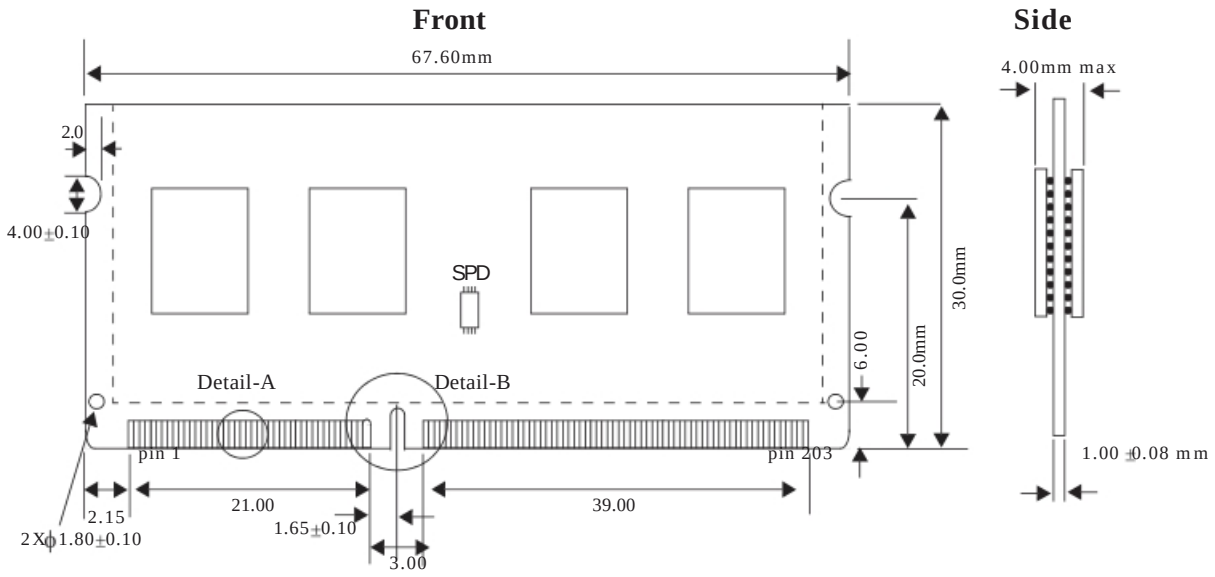
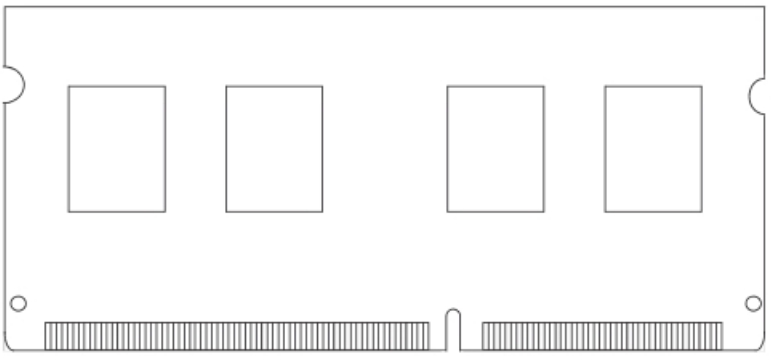
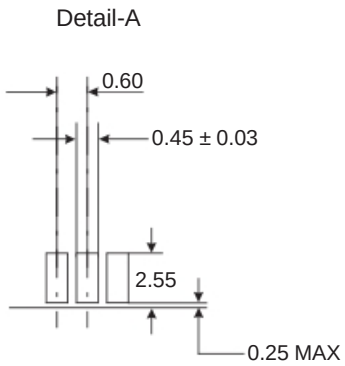
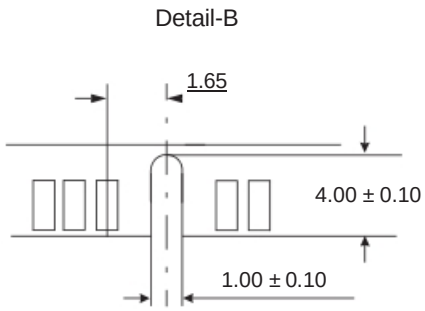
Physical Dimension









Note :

1. +/- 0.13 tolerance on all dimensions unless otherwise stated.

Units: millimeters

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