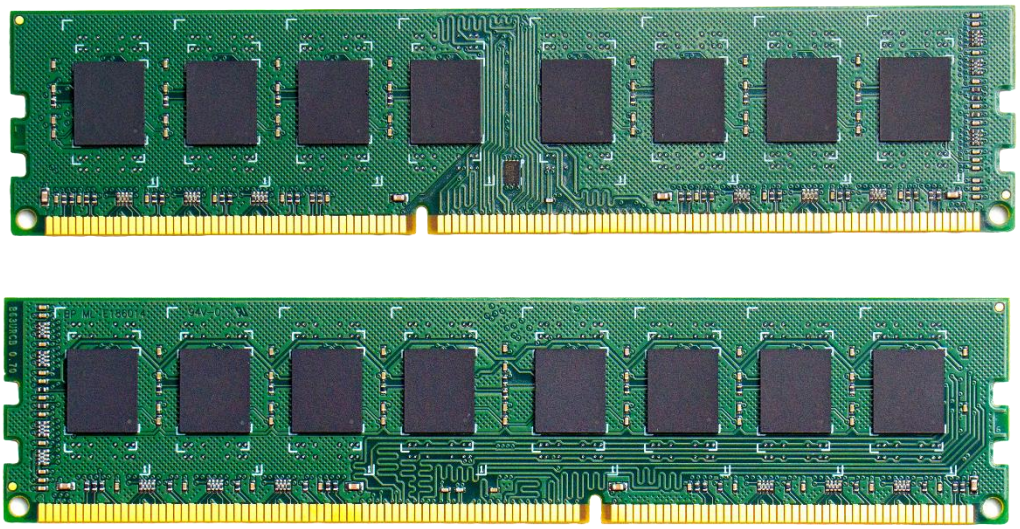
AlfaMemory

8GB DDR3-1600 UB-DIMM 1.35V

240pin PC3-12800 DDR3L Unbuffered DIMM Non-ECC



TEL:+886-3-3465059 FAX:+886-3-3467059
4F., No.890 Jingguo Rd., Luzhu Dist., Taoyuan City 338, Taiwan
AlfaMemory Technology Co., Ltd.

Table of Contents

TEL:+886-3-3465059 FAX:+886-3-3467059
4F., No.890 Jingguo Rd., Luzhu Dist., Taoyuan City 338, Taiwan
AlfaMemory Technology Co., Ltd.

AMC085MADPB8

8G Bytes (1024M x 64 bits)
based on 16 pcs 512M x 8 DDR3L SDRAM
240pin PC3-12800 DDR3L Unbuffered DIMM Non-ECC

Specifications

- RoHS Compliant (Lead Free) Memory module
- Density: 8GB
- Organization
  — 1024M x 64 bits, 2 Rank
- Mounting 16 pieces of 4G bits DDR3L SDRAM sealed In FBGA
- Package: 240-pin socket type Unbuffered dual in line memory module (DIMM)
  — PCB height: 30.00mm
- VDD = 1.35V (1.283V to 1.45V)
- VDDSPD = +3.0V to +3.6V
- Backward Compatible with 1.5V DDR3 Memory module
- Fast Data Transfer Rate: PC3-12800
- Serial Presence-Detect (SPD)with EEPROM
- Eight Internal banks for concurrent operation (components)
- On-Die-Termination (ODT) for better signal quality
- Interface: SSTL_15
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- CAS (READ) latency (CL): 6, 7, 8, 9, 10, 11
- POSTED CAS ADDITIVE latency (AL)
- Precharge: Auto precharge option for each burst access
- Refresh: Auto-refresh, self-refresh
- T_{CASE} of 0°C to 95°C (Components)
  — 64ms, 8,192 cycle refresh at 0°C to 85°C — 32ms at 85°C to 95°C
- Operating Temperature (Tcase)
  — T_{OPR} = 0°C to +85°C
- Fly-by topology

Features

- Double-data-rate architecture; two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted /CAS by progrmmable additive latency for better command and data bus efficiency
- On-Die-Termination (ODT) for better signal quality
  — Synchronous ODT — Dynamic ODT
  — Asynchronous ODT
- Multi Purpose Register (MPR) for temperature read out
- ZQ calibration for DQ drive and ON-Die-Termination
- Progrmmable Partial Array Self-Refresh (PASR)
- /RESET pin for Power-up sequence and reset function • Extended Self-Refresh — External Self-Refresh — Auto Self-Refresh

Key Parameters

MT/s	tCK (ns)	CAS Latency (tCK)	tRCD (ns)	tRP (ns)	tRAS (ns)	tRC (ns)	CL-tRCD-tRP
DDR3-1600	1.25	11	13.125	13.125	35	48.125	11-11-11

TEL:+886-3-3465059 FAX:+886-3-3467059
4F., No.890 Jingguo Rd., Luzhu Dist., Taoyuan City 338, Taiwan
AlfaMemory Technology Co., Ltd.

Pin Descriptions

Pin Name	Description	Pin Name	Description
A[15/14/13:0]	SDRAM address bus	SCL	I2C serial bus clock for EEPROM
BA0-BA2	SDRAM bank select	SDA	I2C serial bus data line for EEPROM
RAS	SDRAM row address strobe	SA0-SA2	I2C serial address select for EEPROM
CAS	SDRAM column address strobe	VDD*	SDRAM core power supply
WE	SDRAM write enable	VDDQ*	SDRAM I/O Driver power supply
S0, S1	DIMM Rank Select Lines	VREFDQ	SDRAM I/O reference supply
CKE0,CKE1	SDRAM clock enable lines	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	On-die termination control lines	VSS	Power supply return (ground)
DQ0 - DQ63	DIMM memory data bus	VDDSPD	Serial EEPROM positive power supply
CB0 - CB7	DIMM ECC check bits	NC	Spare Pins(no connect)
DQS0 - DQS8	SDRAM data strobes (positive line of differential pair)	TEST	Used by memory bus analysis tools (unused on memory DIMMs)
$\overline{\text{DQS}}$0-$\overline{\text{DQS}}$8	SDRAM differential data strobes (negative line of differential pair)	$\overline{\text{RESET}}$	Set DRAMs Known State
DM0-DM8	SDRAM data masks/high data strobes (x8-based x72 DIMMs)	$\overline{\text{EVENT}}$	Reserved for optional temperature-sensing hardware
CK0, CK1	SDRAM clocks (positive line of differential pair)	VTT	SDRAM I/O termination supply
CK0, CK1	SDRAM clocks (negative line of differential pair)	RFU	Reserved for future use

NOTE :
*The VDD and VDDQ pins are tied common to a single power-plane on these designs.
** DQS8, $\overline{\text{DQS}}$8, DM8 arefor ECC UDIMM only

TEL:+886-3-3465059 FAX:+886-3-3467059
4F., No.890 Jingguo Rd., Luzhu Dist., Taoyuan City 338, Taiwan
AlfaMemory Technology Co., Ltd.

Input/Output Functional Descriptions

Symbol	Type	Function
CK0-CK1 CK0-CK1	SSTL	CK and CK are differential clock inputs. All the DDR3 SDRAM addr/cntl inputs are sampled on the crossing of positive edge of CK and negative edge of CK. Output (read) data is reference to the crossing of CK and CK (Both directions of crossing)
CKE0-CKE1	SSTL	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self-Refresh mode
$\overline{S}$0-$\overline{S}$1	SSTL	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new command are ignored but previous operations continue. This signal provides for external rank selection on systems with multiple ranks.
$\overline{RAS}$, $\overline{CAS}$, WE	SSTL	$\overline{RAS}$, $\overline{CAS}$, and WE (ALONG WITH S) define the command being entered.
ODT0-ODT1	SSTL	When high, termination resistance is enabled for all DQ, DQS, DQS and DM pins, assuming the function is enabled in the Extended Mode Register Set (EMRS).
V_{REFDQ}	Supply	Reference voltage for SSTL 15 I/O inputs.
V_{REFCA}	Supply	Reference voltage for SSTL 15 command/address inputs.
V_{DDQ}	Supply	Power supply for the DDR3 SDRAM output buffers to provide improved noise immunity. For all current DDR3 unbuffered DIMM designs, V_{DDQ} shares the same power plane as V_{DD} pins.
BA0-BA2	SSTL	Selects which SDRAM bank of eight is activated.
A[15/14/13:0]	SSTL	During a Bank Activate command cycle, Address input defines the row address (RA0-RA13) During a Read or Write command cycle, Address input defines the column address, In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1, BA2 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a pre-charge command cycle, AP is used in conjunction with BA0, BA1, BA2 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0, BA1 or BA2. If AP is low, BA0, BA1 and BA2 are used to define which bank to precharge. A12(BC) is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH, no burst chop; Low, burst chopped).
DQ0-DQ63 CB0-CB7	SSTL	Data and Check Bit Input/Output pins.
DM0-DM8[1]	SSTL	DM is an input mask signal for write data. Input data is masked when DM is sampled High coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
V_{DD},V_{SS}	Supply	Power and ground for DDR3 SDRAM input buffers, and core logic. V_{DD} and V_{DDQ} pins are tied to V_{DD}/V_{DDQ} planes on these modules.
0-DQS8[1] $\overline{0}$-DQS8[1]	SSTL	Data strobe for input and output data.
SA0-SA2	-	These signals and tied at the system planar to either V_{SS} or V_{DDSPD} to configure the serial SPD EERPOM address range.
SDA	-	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. An external resistor may be connected from the SDA bus line to V_{DDSPD} to act as a pull-up on the system board.
SCL	-	This signal is used to clock data into and out of the SPD EEPROM. An external resistor may be connected from the SCL bus time to V_{DDSPD} to act as a pull-up on the system board.
V_{DDSPD}	Supply	Power supply for SPD EEPROM. This supply is separate from the V_{DD}/V_{DDQ} power plane. EEPROM supply is operable from 3.0V to 3.6V.
RESET	-	The RESET pin is connected to the RESET pin on each DRAM. When low, all DRAMs are set to a know state.
$\overline{EVENT}$	Output	This signal indicates that a thermal event has been detected in the thermal sensing device. The system should guarantee the electrical level requirement is met for the EVENT pin on TS/SPD part

NOTE :
1. DM8, DQS8 and $\overline{DQS}$8 are for ECC UDIMM only.

TEL:+886-3-3465059 FAX:+886-3-3467059
4F., No.890 Jingguo Rd., Luzhu Dist., Taoyuan City 338, Taiwan
AlfaMemory Technology Co., Ltd.

Pin Configurations

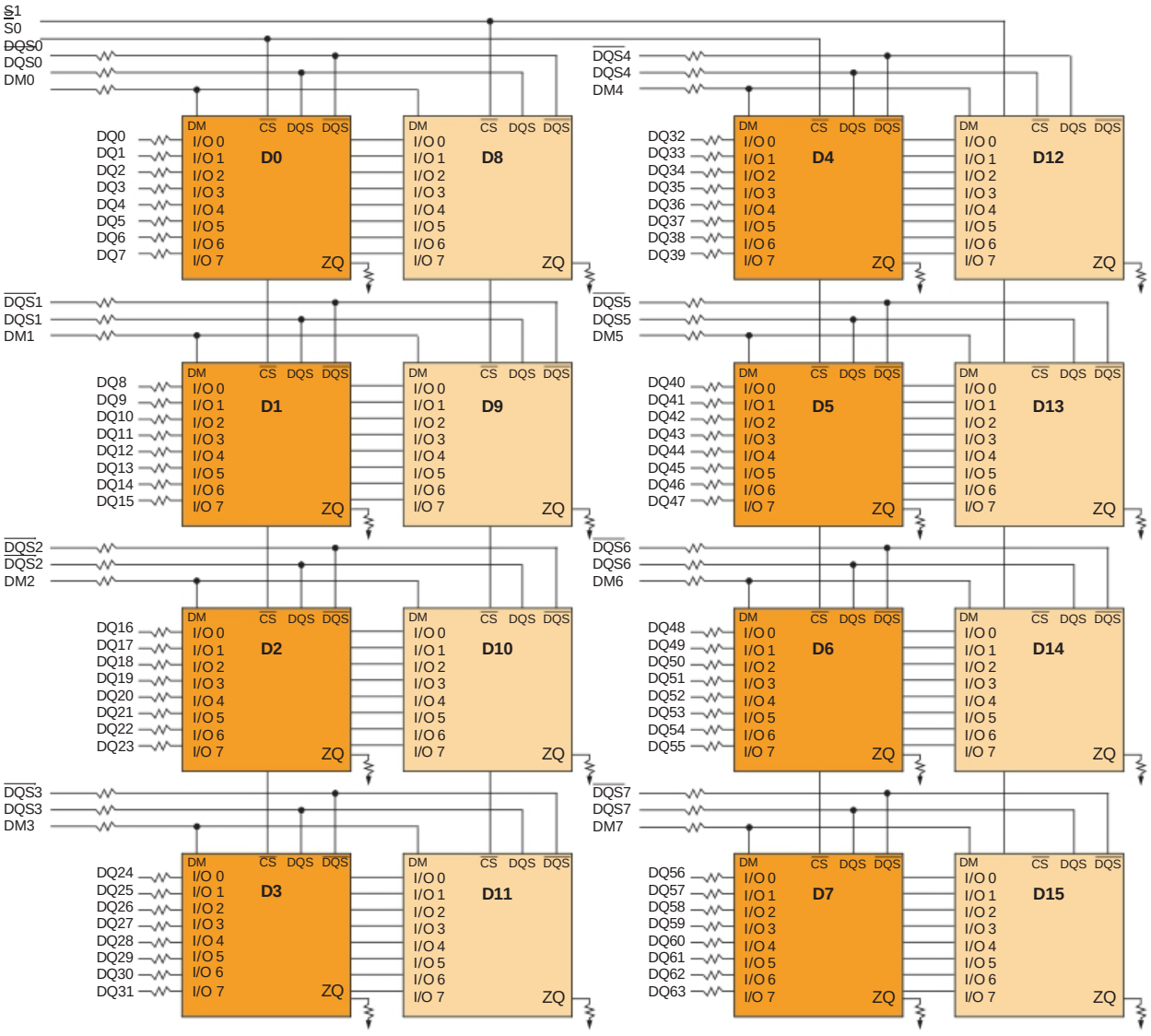
Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VREFDQ	121	VSS	42	NC	162	NC	82	DQ33	202	VSS
2	VSS	122	DQ4	43	NC	163	VSS	83	VSS	203	DM4
3	DQ0	123	DQ5	44	VSS	164	NC	84	DQS4	204	NC
4	DQ1	124	VSS	45	NC	165	NC	85	DQS4	205	VSS
5	VSS	125	DM0	46	NC	166	VSS	86	VSS	206	DQ38
6	DQS0	126	NC	47	VSS	167	NC (TEST)3	87	DQ34	207	DQ39
7	DQS0	127	VSS	48	NC	168	Reset	88	DQ35	208	VSS
8	VSS	128	DQ6	KEY				89	VSS	209	DQ44
9	DQ2	129	DQ7	49	NC	169	CKE1,NC1	90	DQ40	210	DQ45
10	DQ3	130	VSS	50	CKE0	170	VDD	91	DQ41	211	VSS
11	VSS	131	DQ12	51	VDD	171	A15,NC	92	VSS	212	DM5
12	DQ8	132	DQ13	52	BA2	172	A14,NC	93	DQS5	213	NC
13	DQ9	133	VSS	53	NC	173	VDD	94	DQS5	214	VSS
14	VSS	134	DM1	54	VDD	174	A12/BC	95	VSS	215	DQ46
15	DQS1	135	NC	55	A11	175	A9	96	DQ42	216	DQ47
16	DQS1	136	VSS	56	A7	176	VDD	97	DQ43	217	VSS
17	VSS	137	DQ14	57	VDD	177	A8	98	VSS	218	DQ52
18	DQ10	138	DQ15	58	A5	178	A6	99	DQ48	219	DQ53
19	DQ11	139	VSS	59	A4	179	VDD	100	DQ49	220	VSS
20	VSS	140	DQ20	60	VDD	180	A3	101	VSS	221	DM6
21	DQ16	141	DQ21	61	A2	181	A1	102	DQS6	222	NC
22	DQ17	142	VSS	62	VDD	182	VDD	103	DQS6	223	VSS
23	VSS	143	DM2	63	CK1,NC	183	VDD	104	VSS	224	DQ54
24	DQS2	144	NC	64	CK1,NC	184	CK0	105	DQ50	225	DQ55
25	DQS2	145	VSS	65	VDD	185	CK0	106	DQ51	226	VSS
26	VSS	146	DQ22	66	VDD	186	VDD	107	VSS	227	DQ60
27	DQ18	147	DQ23	67	VREFCA	187	NC	108	DQ56	228	DQ61
28	DQ19	148	VSS	68	NC	188	A0	109	DQ57	229	VSS
29	VSS	149	DQ28	69	VDD	189	VDD	110	VSS	230	DM7
30	DQ24	150	DQ29	70	A10/AP	190	BA1	111	DQS7	231	NC
31	DQ25	151	VSS	71	BA0	191	VDD	112	DQS7	232	VSS
32	VSS	152	DM3	72	VDD	192	RAS	113	VSS	233	DQ62
33	DQS3	153	NC	73	WE	193	S0	114	DQ58	234	DQ63
34	DQS3	154	VSS	74	CAS	194	VDD	115	DQ59	235	VSS
35	VSS	155	DQ30	75	VDD	195	ODT0	116	VSS	236	VDDSPD
36	DQ26	156	DQ31	76	S1, NC1	196	A13	117	SA0	237	SA1
37	DQ27	157	VSS	77	ODT1, NC1	197	VDD	118	SCL	238	SDA
38	VSS	158	NC	78	VDD	198	NC	119	SA2	239	VSS
39	NC	159	NC	79	NC	199	VSS	120	VTT	240	VTT
40	NC	160	VSS	80	VSS	200	DQ36				
41	VSS	161	NC	81	DQ32	201	DQ37				

NOTE : NC = No Connect; NU = Not Used; RFU = Reserved Future Use

1. S1, ODT1, CKE1: Used for dual-rank UDIMMs; NC on single-rank UDIMMs
2. CK1,NC and CK1,NC : Used for dual-rank UDIMMs; not used on single-rank UDIMMs, but terminated
3. TEST (pin 167) used by memory bus analysis tools (unused on memory DIMMs)

TEL:+886-3-3465059 FAX:+886-3-3467059
4F., No.890 Jingguo Rd., Luzhu Dist., Taoyuan City 338, Taiwan
AlfaMemory Technology Co., Ltd.

Functional Block Diagram



BA0 - BA2 → BA0-BA2 : SDRAMs D0 - D15

A[15/14/13:0] → A[15/14/13:0] : SDRAMs D0 - D15

CKE1 → CKE : SDRAMs D8 - D15

CKE0 → CKE : SDRAMs D0 - D7

$\overline{RAS}$ → $\overline{RAS}$: SDRAMs D0 - D15

$\overline{CAS}$ → $\overline{CAS}$: SDRAMs D0 - D15

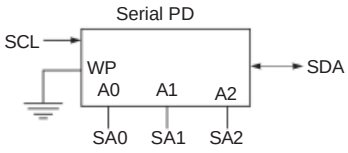
$\overline{WE}$ → $\overline{WE}$: SDRAMs D0 - D15

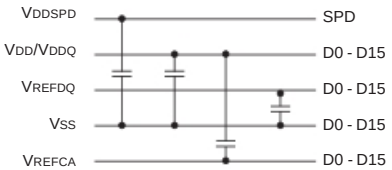
ODT0 → ODT : SDRAMs D0 - D7

ODT1 → ODT : SDRAMs D8 - D15

CK0 → CK : SDRAMs D0 - D7

CK1 → CK : SDRAMs D8 - D15



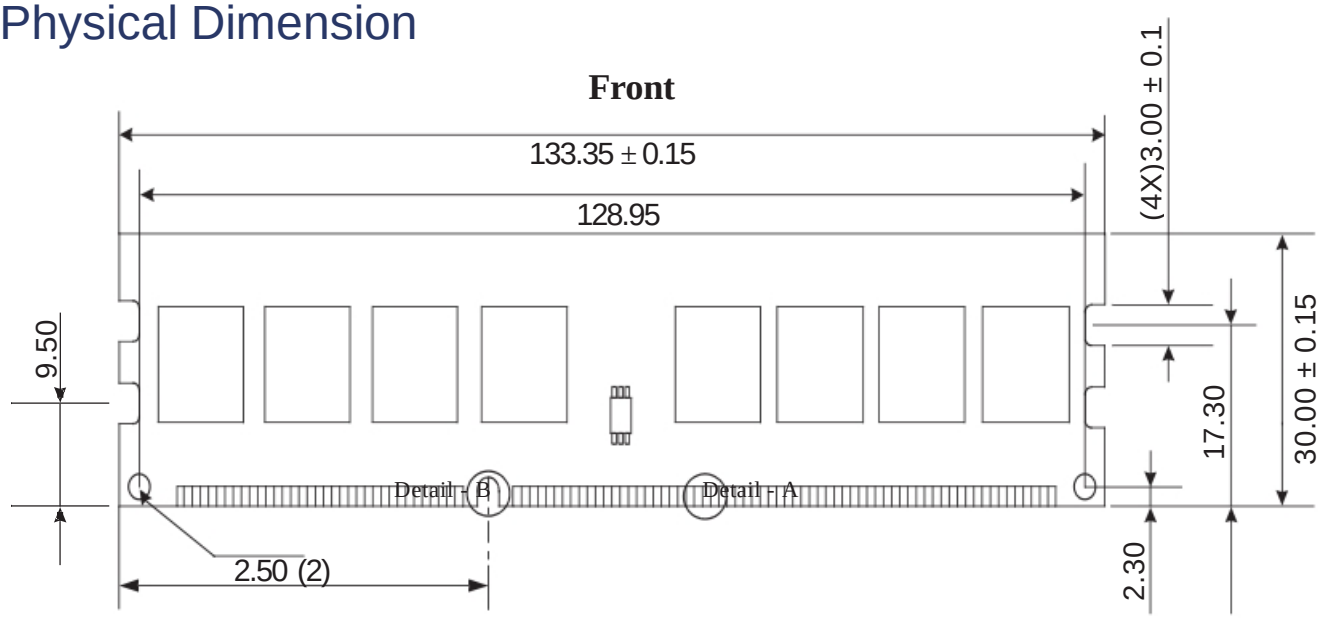


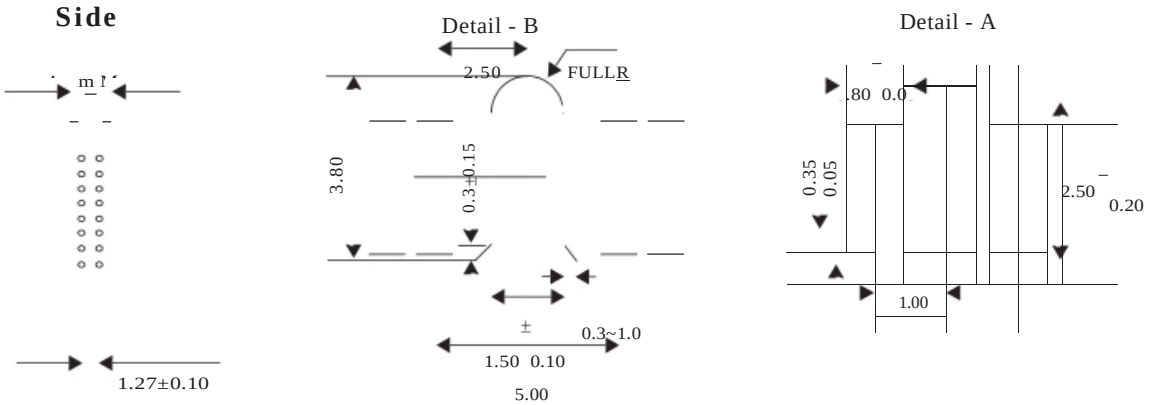
NOTE :

1. For each DRAM, a unique ZQ resistor is connected to ground. The ZQ resistor is 240 Ohm +/- 1%
2. One SPD exists per module.

TEL:+886-3-3465059 FAX:+886-3-3467059
4F., No.890 Jingguo Rd., Luzhu Dist., Taoyuan City 338, Taiwan
AlfaMemory Technology Co., Ltd.

Physical Dimension





Note:

1. 0.15 tolerance on all dimensions unless otherwise stated.

Units: millimeters

TEL:+886-3-3465059 FAX:+886-3-3467059
4F., No.890 Jingguo Rd., Luzhu Dist., Taoyuan City 338, Taiwan
AlfaMemory Technology Co., Ltd.